

## CLAIMS

What is claimed is:

- 1     1.     A multiplier circuit, comprising:  
2             at least one Booth encoder circuit to encode a plurality of multiplier bits into  
3     four encoded outputs, the encoded outputs to select Booth-multiply functions; and  
4             a plurality of multiplexer circuits, one multiplexer circuit for each bit of the  
5     multiplicand, at least one of the plurality multiplexer circuits including four pass  
6     gates coupled to receive a multiplicand bit, a complement of the multiplicand bit,  
7     multiplexed data from a next lower order multiplexer circuit and the encoded  
8     outputs of the Booth encoder circuit to provide one bit of a partial product at a  
9     multiplexer output.
- 1     2.     The multiplier circuit of claim 1, wherein the four encoded outputs select  
2     Booth-multiply functions which include negative, positive, zero, multiply by one  
3     and multiply by two.
- 1     3.     The multiplier circuit of claim 1, wherein the multiplier circuit includes  $M/2$   
2     Booth encoder circuits each coupled to a plurality of multiplexer circuits, each  
3     Booth encoder circuit receiving three bits of an  $M$ -bit multiplier to output  $M/2$   
4     Booth-multiply partial products.
- 1     4.     The multiplier circuit of claim 3, wherein the multiplier circuit further  
2     includes an adder circuit coupled to the outputs of the multiplexers to add the partial  
3     products and obtain a product of the multiply operation.
- 1     5.     The multiplier circuit of claim 3 further including a  $N$ -bit multiplicand,  
2     wherein  $M$  and  $N$  are integers selectable from one or a combination of sixteen,  
3     thirty-two and sixty-four.

1     6.     The multiplier of claim 1, wherein the Booth encoder circuit includes at least  
2     one fanout driver circuit to drive at least one select output and the outputs of the  
3     multiplexer circuits include fanout drivers to drive the partial product bits.

1     7.     The multiplier circuit of claim 6, wherein the fanout drivers include  
2     inverters.

1     8.     A plurality of multiplexer circuits, each multiplexer circuit including four  
2     transistors, the transistors coupled to receive Booth encoded signals, a multiplicand  
3     bit, a complement of the multiplicand bit, and at least one of the multiplexer circuits  
4     coupled to receive multiplexed data from a next lower order multiplexer circuit,  
5     wherein one bit of a partial product is selected for output from the at least one  
6     multiplexer circuit according to the Booth encoded signals.

1     9.     The circuit of claim 8, wherein the four transistors include:

2             first and second transistors, the gates of the transistors coupled to receive a  
3     multiplicand bit and its complement, a first source/drain region of the transistors  
4     coupled to receive first and second Booth encoded signals and a second source/drain  
5     region of the transistors coupled together and coupled to the input of a next higher  
6     order multiplexer, the coupled second source/drain regions to provide a positive or a  
7     negative multiplicand bit according to the first and second Booth encoded signals;  
8     and

9             a third transistor, a first source/drain region of the third transistor coupled to  
10    the second source/drain regions of the first and second transistors, the gate of the  
11    third transistor coupled to receive a third Booth encoded signal, and a second  
12    source/drain region of the third transistor providing an output corresponding to one  
13    bit of a partial product; and

14            a fourth transistor, a first source/drain region of the fourth transistor to  
15    receive multiplexed data from a next lower order multiplexer; the gate of the fourth  
16    transistor to receive a fourth Booth encoded signal, a second source/drain region of

17 the fourth transistor coupled to the second source/drain region of the third transistor,  
18 the coupled second source/drain regions to provide one bit of a partial product  
19 according to the third and fourth Booth encoded signals.

1 10. The circuit of claim 8, wherein the Booth encoded signals include four  
2 Booth encoded signals encoded from three bits of a multiplier and which select  
3 Booth-multiply functions that include negative, positive, multiply by two and  
4 multiply by one.

1 11. The circuit of claim 10, wherein a multiplexer output is zero when both the  
2 positive and negative result signals are low.

1 12. The circuit of claim 8, wherein a delay from a multiplicand bit to an output  
2 of the circuit is a maximum of two transistor delays.

1 13. The circuit of claim 8, wherein the transistors include NFET transistors.

1 14. A Booth encoder circuit comprising:  
2 a plurality of logic circuits to generate control signals used to generate  
3 Booth-multiply partial products, the logic circuits only including:  
4 a first logic circuit to generate a signal for a negative partial product;  
5 a second logic circuit to generate a signal for a positive partial  
6 product;  
7 a third logic circuit to generate a signal to multiply a multiplicand by  
8 two; and  
9 a fourth logic circuit to generate a signal to multiply a multiplicand by one.

1 15. The circuit of claim 14, wherein the Booth encoder circuit generates a zero  
2 partial product when outputs of the first and second logic circuits are both low.

1 16. The circuit of claim 14, wherein inputs to the logic circuits include bits of a  
2 multiplier and complements of the bits of a multiplier.

1 17. The circuit of claim 16, wherein the first logic circuit comprises:  
2 a two-input NAND gate, wherein the inputs to the NAND gate are first and  
3 second bits of a multiplier;  
4 a T-gate coupled to the output of the NAND gate, wherein a third multiplier  
5 bit and a complement of the third multiplier bit activate the T-gate, and wherein the  
6 output of the T-gate includes the signal for a negative partial product; and  
7 a pull-down transistor coupled to the output T-gate, wherein the complement of the  
8 third multiplier bit activates the pull down transistor.

1 18. The circuit of claim 16, wherein the first logic circuit comprises:  
2 a fifth logic circuit that is high when first, second and third bits of a  
3 multiplier are not all ones or all zeros; and  
4 a two-input AND gate, wherein a first input to the AND gate is the output of the  
5 fifth logic circuit and a second input is the third bit of a multiplier.

1 19. The circuit of claim 16, wherein the second logic circuit comprises:  
2 a two-input NAND gate, wherein the inputs to the NAND gate are  
3 complements of first and second bits of a multiplier;  
4 a T-gate coupled to the output of the NAND gate, wherein a third multiplier  
5 bit and a complement of the third multiplier bit activate the T-gate, and wherein the  
6 output of the T-gate includes a signal for the positive partial product; and  
7 a pull-down transistor coupled to the output T-gate, wherein the third multiplier bit  
8 activates the pull down transistor.

1 20. The circuit of claim 16, wherein the second logic circuit comprises:  
2 a fifth logic circuit that is high when first, second and third bits of a  
3 multiplier are not all ones or all zeros; and

4 a two-input AND gate, wherein a first input to the AND gate is the output of the  
5 fifth logic circuit and a second input is a complement of the third bit of a multiplier.

1 21. The circuit of claim 16, wherein the third logic circuit comprises a two-input  
2 XOR gate, wherein the inputs to the XOR gate are first and second bits of a  
3 multiplier and the output of the XOR gate is the signal to multiply a multiplicand by  
4 one.

1 22. The circuit of claim 16, wherein the fourth logic circuit comprises a two-  
2 input XNOR gate, wherein the inputs to the XNOR gate are first and second bits of  
3 a multiplier and the output of the XNOR gate is the signal to multiply a multiplicand  
4 by two.

1 23. A method of multiplying comprising:  
2 generating four control signals to implement Booth encoding functions of  
3 negative, positive, zero, multiply by one and multiply by two, from bits of a  
4 multiplier;  
5 multiplexing bits of a multiplicand in accordance with the control signal  
6 functions to generate partial products, wherein multiplexing includes  
7 interconnecting intermediate stages of multiplexers from lower order bit positions to  
8 next higher order positions; and  
9 adding the partial products to obtain the final product.

1 24. The method of claim 23, wherein multiplexing includes distributing the  
2 multiplicand bits to create a maximum delay of two transistors from a multiplicand  
3 bit to an output of the circuit.

1 25. The method of claim 23, wherein generating control signals includes  
2 generating the zero function signal when the negative and positive function signals  
3 are both low.

1 26. The method of claim 23, wherein multiplexing to generate partial products  
2 includes simultaneously generating  $M/2$  partial products for an M-bit multiplier.

1 27. The method of claim 23, wherein multiplexing to generate partial products  
2 includes generating one partial product, and adding includes accumulating a sum of  
3 the partial products as the partial products are generated.

1 28. A computer system comprising:  
2 a bus that communicates information;  
3 a memory coupled to the bus, the memory to store a multiply instruction;  
4 and  
5 a processor coupled to the bus, the processor to process information, the  
6 processor including a multiplier circuit, the multiplier circuit including at least one  
7 partial product generator, wherein the at least one partial product generator includes:  
8 a Booth encoder circuit to encode a plurality of multiplier bits into  
9 four encoded outputs, the encoded outputs to select Booth-multiply  
10 functions; and  
11 a plurality of multiplexer circuits, one multiplexer circuit for each bit  
12 of the multiplicand, at least one of the plurality of multiplexer circuits  
13 including:  
14 four pass gates, the pass gates coupled to a multiplicand bit, a complement  
15 of the multiplicand bit, multiplexed data from a next lower order multiplexer circuit  
16 and the Booth encoder circuit outputs, the Booth encoder circuit outputs to enable  
17 one or a combination of the pass gates to provide one bit of a partial product at a  
18 multiplexer output.

1 29. The computer system of claim 28, wherein the Booth encoder select outputs  
2 to enable the functions positive, negative, zero, multiply by one and multiply by  
3 two.

1     30.     The computer system of claim 29, wherein the multiplier circuit implements  
2     a sixty-four by sixty-four bit multiply.